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EXAMINER
HSU, JONI

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,524	LEE, HIN-KWAI	
	Examiner	Art Unit	
	Joni Hsu	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *17* is/are withdrawn from consideration.

5)☒ Claim(s) *15,16 and 18-20* is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments filed January 12, 2005 have been fully considered but they are not persuasive.

2. Applicant states that the heading on the Claim section is being amended as requested by the Examiner (page 12, line 6). Therefore, the objection on the specification is withdrawn.

3. Applicant has added the limitation of a frame-buffer extension in the DRAM to independent claims 1, 10, and 15. This limitation was cited by the Examiner as allowable subject matter. In view of this, Applicant submitted that claims 1-16 and 18-20, as amended, are in position for allowance (page 12, lines 10-15).

In reply, the Examiner disagrees. In the "Background of Invention" section of the specification of this application, it is stated that extensions in DRAM may be needed when the frame buffer is larger than the available space in SRAM [0005]. "Background of Invention" sections typically discuss prior art related to the invention. Therefore, it appears that Applicant has admitted that a frame-buffer extension in the DRAM has been used in prior art. Therefore this limitation is rejected, and therefore, claims 1-16 and 18-20 stand rejected.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of Applicant's Admitted Prior Art (APA), Paragraphs [0001] to [0008].

7. With regard to Claim 1, Schlapp describes a graphics system comprising a dynamic-random-access memory (DRAM) for storing graphics data (Col. 4, lines 41-51); a static random-access memory (SRAM) (56, Figure 2) for storing pixels in a frame buffer (Col. 4, lines 59-61); a first bus to the SRAM (pixel operation bus, 112); a second bus to the DRAM (DRAM

operation bus, 110); a refresh controller (340, Figure 3; Col. 13, lines 55-63), which is coupled to the SRAM through the arbiter (330) and the first bus (pixel operation bus) (Col. 14, lines 5-9), and coupled to the DRAM through the arbiter and the second bus (DRAM operation bus) (Col. 13, line 64-Col. 14, line 5), for reading pixels from the frame buffer for display to a display device; a graphics engine (70), coupled to the SRAM through the first bus, and coupled to the DRAM through the second bus, for reading and writing graphics data (Col. 3, line 60-Col. 4, line 19); and a dual-layer arbiter (330, Figure 3), receiving requests from the refresh controller to access the SRAM and requests from the graphics engine to access the DRAM, and also receiving requests from the refresh controller to access the DRAM and requests from the graphics engine to access the SRAM (Col. 13, line 55-Col. 14, line 9), the dual-layer arbiter allowing simultaneous access of the DRAM and SRAM (Col. 17, lines 20-26) when the refresh controller requests access of the SRAM (Col. 2, lines 8-12; Col. 4, lines 27-35) and the graphics engine requests access of the DRAM (Col. 3, line 60-Col. 4, line 19), but the dual-layer arbiter delaying access of the DRAM by the graphics engine when the refresh controller access the DRAM, whereby the dual-layer arbiter allows simultaneous DRAM and SRAM access or arbitrated access of either the DRAM or the SRAM (Col. 17, lines 39-53).

However, Schlapp does not teach a frame-buffer extension in the DRAM, the frame-buffer extension for storing pixels read by the refresh controller for larger frame buffers. However, in the "Background of Invention" section of the specification of this application, it is stated that extensions in DRAM may be needed when the frame buffer is larger than the available space in SRAM [0005]. "Background of Invention" sections typically discuss prior art

related to the invention. Therefore, it appears that Applicant has admitted that a frame-buffer extension in the DRAM has been used in prior art.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Schlapp to include a frame-buffer extension in the DRAM, the frame-buffer extension for storing pixels read by the refresh controller for larger frame buffers as suggested by APA because APA suggests that extensions may be needed when the frame buffer is larger than the available space in SRAM [0005].

8. With regard to Claim 3, Schlapp describes that the SRAM has a higher speed than the DRAM (Col. 4, lines 59-61), and therefore has a smaller access time.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of APA [0001-0008], further in view of Yamashita (US006313844B1).

Schlapp and APA are relied upon for the teachings as discussed above relative to Claim 1. Schlapp describes a SRAM (56, Figure 2; Col. 3, lines 26-29), and the SRAM inherently stores data as states of a bi-stable circuit. This is inherent because all SRAM devices store data as states of a bi-stable circuit, according to the definition found on the free-definition website.

However, Schlapp and APA do not teach that the DRAM stores data as charges on capacitors that periodically require refreshing of the charges. However, Yamashita describes a graphics system comprising a DRAM (16, Figure 9; Col. 14, lines 18-21), a SRAM (17; Col. 15, lines 8-19), a refresh controller (30; Col. 16, lines 41-45), and a graphics engine (12; Col. 15,

lines 24-31). Yamashita describes that the DRAM stores data as charges on capacitors that periodically require refreshing of the charges (Col. 1, lines 37-43).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Schlapp and APA so that the DRAM stores data as charges on capacitors that periodically require refreshing of the charges as suggested by Yamashita because Yamashita suggests that all DRAM devices store data in this manner (Col. 1, lines 37-43). This is well-known in the art.

10. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of APA [0001-0008], further in view of Rodgers (US006131140A).

11. With regard to Claim 4, Schlapp and APA are relied upon for the teachings as discussed above relative to Claim 3. Schlapp describes that the first bus (112, Figure 1) is coupled to the refresh controller (340, Figure 3; Col. 2, lines 8-12; Col. 4, lines 27-35; Col. 13, lines 55-63; Col. 14, lines 5-9) and the graphics engine (70, Figure 1; Col. 3, line 60-Col. 4, line 19) and the second bus (110) is coupled to the refresh controller (Col. 4, lines 27-35; Col. 13, line 64-Col. 14, line 5) and the graphics engine (Col. 3, line 60-Col. 4, line 19). Schlapp describes a dual-layer arbiter (330, Figure 3), receiving requests from the refresh controller to access the SRAM and requests to access the DRAM, and also receiving requests from the graphics engine to access the DRAM and requests to access the SRAM (Col. 13, line 55-Col. 14, line 9).

However, Schlapp and APA do not teach a first mux and a second mux for connecting the SRAM and the DRAM to the refresh controller and the graphics engine. However, Rodgers

describes a first mux (201a, Figure 3a) connecting the SRAM (105a) to other components (Col. 6, line 66-Col. 7, line 4) and a second mux (208) connecting the DRAM (109, Figure 2) to other components (Col. 8, lines 39-46).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Schlapp and APA to include a first mux and a second mux for connecting the SRAM and the DRAM to the refresh controller and the graphics engine as suggested by Rodgers. A multiplexer is a device for taking several separate digital data streams and combining them together into one data stream of a higher data rate. Multiplexers have the advantage of allowing multiple data streams to be carried from one place to another over one physical link, which saves cost. Multiplexers are well-known in the art, widely used, and can be found in many publications, such as the *Wikipedia Encyclopedia*.

12. With regard to Claim 5, Schlapp describes that the first bus can transfer data to the SRAM at a same time that the second bus transfers data to the DRAM, as discussed in the rejection for Claim 1.

However, Schlapp does not teach a first mux and a second mux. However, Rodgers describes a first mux and a second mux, as discussed in the rejection for Claim 4.

13. With regard to Claim 6, Schlapp describes that the first bus (112, Figure 1) comprises address and control signals for controlling access to the SRAM (56, Figure 2; Col. 3, lines 26-29); wherein the second bus (110, Figure 1) comprises address and control signals for controlling access to the DRAM (Col. 3, lines 21-25) (Col. 4, lines 27-35). Schlapp describes a separate bus

(98, Figure 2) for providing data to the SRAM and the DRAM (Col. 4, lines 7-19). However, it would be obvious to include data lines in buses 110 and 112 because as can be seen in Figure 2, buses 110 and 112 contain many different signals, so it would be obvious to include the data signal in these buses as well.

14. With regard to Claim 7, Schlapp describes a SRAM (56, Figure 2) for storing graphics data read by the graphics engine (70) (Col. 13, line 55-Col. 14, line 9), as discussed in the rejection for Claim 1.

However, Schlapp does not teach a buffer extension, in the SRAM, for storing graphics data read by the graphics engine. However, the "Background of Invention" section of the specification of this application discusses the use of buffer extensions [0005], as discussed in the rejection for Claim 1.

15. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of APA [0001-0008], further in view of Rodgers (US006131140A), further in view of Laksono (US006288729B1).

Schlapp, APA, and Rodgers are relied upon for the teachings as discussed above relative to Claim 4. Schlapp describes that the dual-layer arbiter allows simultaneous access of the DRAM and SRAM when the refresh controller requests access of the SRAM and the graphics engine requests access of the DRAM, but the dual-layer arbiter delaying access of the DRAM by the graphics engine when the refresh controller access the DRAM, as discussed in the rejection for Claim 1. Rodgers describes a first mux (201a, Figure 3a) connecting the SRAM (105a) to

other components (Col. 6, line 66-Col. 7, line 4) and a second mux (208) connecting the DRAM (109, Figure 2) to other components (Col. 8, lines 39-46), as discussed in the rejection for Claim 4.

However, Schlapp, APA, and Rodgers do not teach a second graphics engine. However, Laksono describes a second graphics engine (plurality of clients, clients are graphics engines, Col. 5, lines 57-62) coupled to the graphics memory (20, Figure 1) through the first bus shown in Figure 1, and computed to the system memory (16) through the second bus (22), for reading and writing graphics data; wherein the dual-layer arbiter (26) further receives requests from the second graphics engine to access the system memory, and requests from the second graphics engine to access the graphics memory (Col. 4, lines 35-38), and the dual-layer arbiter is connected to the second graphics engine, the system memory, and the graphics memory (Col. 4, lines 35-38).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Schlapp, APA, and Rodgers to include a second graphics engine as suggested by Laksono because Laksono suggests the advantage of multiple graphics engines being able to share the same memory, making more use out of the memory (Col. 2, lines 4-9). It also would have been obvious to modify the device of Rodgers so that the muxes are able to be connected to the second graphics engine. For example, Rodgers describes that mux 208 is a 2 to 1 mux and it connects the PCI bus to the DRAM (Col. 8, lines 39-42). However, 3 to 1 muxes are also well-known in the art, so it would have been obvious to modify mux 208 to make it a 3 to 1 mux so that the second graphics engine can also be connected to the second graphics engine.

16. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A), in view of APA [0001-0008], further in view of Rodgers (US006131140A), further in view of Laksono (US006288729B1), further in view of Lavelle (US006812929B2).

Schlapp, APA, Rodgers, and Laksono are relied upon for the teachings as discussed above relative to Claim 8.

However, Schlapp, APA, Rodgers, and Laksono do not teach that the graphics engine is a video overlay engine or a 3-dimensional graphics engine. However, Lavelle is similar to Schlapp and has a DRAM (914, Figure 8) for storing graphics data and a SRAM (930) for storing pixels in a frame buffer (Col. 10, lines 47-49). Lavelle also describes that the graphics engine is a video overlay engine (190, Figure 6; Col. 9, lines 33-38).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Schlapp, APA, Rodgers, and Laksono so that the graphics engine is a video overlay engine as suggested by Lavelle. A video overlay engine is needed in order to place a full-motion video window on the display screen. Video overlay engines are well-known in the art, widely used, and found in many publications, such as the *Webopedia Computer Dictionary.*

17. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of APA [0001-0008], further in view of Lavelle (US006812929B2), further in view of Rodgers (US006131140A).

Schlapp describes a dual-layer arbitrated graphics system comprising a dynamic-random-access memory (DRAM) for storing graphics data (Col. 3, lines 21-25); a static random-access memory (SRAM) (56, Figure 2) for storing display pixels in a frame buffer (Col. 3, lines 26-29); an SRAM bus (112, Figure 1) for transferring data to and from the SRAM; a DRAM bus (110) for transferring data to and from the DRAM (Col. 4, lines 27-35); a refresh controller (340, Figure 3) coupled to drive display pixels to a display (Col. 2, lines 8-12). Schlapp describes that the first bus (112, Figure 1) is coupled to the refresh controller (340, Figure 3; Col. 2, lines 8-12; Col. 4, lines 27-35; Col. 13, lines 55-63; Col. 14, lines 5-9) and the graphics engine (70, Figure 1; Col. 3, line 60-Col. 4, line 19) and the second bus (110) is coupled to the refresh controller (Col. 4, lines 27-35; Col. 13, line 64-Col. 14, line 5) and the graphics engine (Col. 3, line 60-Col. 4, line 19). Schlapp describes a dual-layer arbiter (330, Figure 3), receiving requests from the refresh controller to access the SRAM and requests to access the DRAM, and also receiving requests from the graphics engine to access the DRAM and requests to access the SRAM (Col. 13, line 55-Col. 14, line 9). Schlapp describes a dual-layer arbiter (330, Figure 3) is coupled to receive requests from the refresh controller (340; Col. 13, lines 55-63) and requests from the graphics engine (102), for arbitrating access to the SRAM (56, Figure 2; Col. 4, lines 59-61) when both the refresh controller and the graphics engine request access to the SRAM, and for arbitrating access to the DRAM (Col. 3, line 60-Col. 4, line 19), but allowing simultaneous or parallel access to both the SRAM and to the DRAM when the refresh controller and the graphics engine request access to different memories; wherein the dual-layer arbiter generates the first select signal to the SRAM and the second select signal to the DRAM in response to the dual-layer arbiter arbitrating access or allowing parallel access (Col. 17, lines 20-26), whereby parallel

access to the SRAM and to the DRAM is allowed when arbitrating access is not required by requests (Col. 17, lines 39-53),

However, Schlapp does not teach a frame-buffer extension in the DRAM, the frame-buffer extension for storing pixels read by the refresh controller. However, in the "Background of Invention" section of the specification of this application, it is stated that extensions in DRAM may be needed when the frame buffer is larger than the available space in SRAM [0005], as discussed in the rejection for Claim 1.

However, Schlapp and APA do not teach that the graphics engine is a first overlay engine. However, Lavelle describes a DRAM (914, Figure 8) for storing graphics data, a SRAM (930) for storing display pixels in a frame buffer (Col. 10, lines 47-49) as discussed in the rejection for Claims 1 and 9, and a first overlay engine (190, Figure 6) that manipulates graphics data (Col. 9, lines 33-38), as discussed in the rejection for Claim 9.

However, Schlapp, APA, and Lavelle do not teach a first mux and a second mux for connecting the SRAM and the DRAM to the refresh controller and the first overlay engine. However, Rodgers describes a first mux (201a, Figure 3a) connecting the SRAM (105a) to other components (Col. 6, line 66-Col. 7, line 4) and a second mux (208) connecting the DRAM (109, Figure 2) to other components (Col. 8, lines 39-46), as discussed in the rejection for Claim 4.

18. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of APA [0001-0008], further in view of Lavelle (US006812929B2), further in view of Rodgers (US006131140A), further in view of Kotzur (US006389480B1).

19. With regard to Claim 11, Schlapp, APA, Lavelle, and Rodgers are relied upon for the teachings as discussed above relative to Claim 10.

However, Schlapp, APA, Lavelle, and Rodgers do not teach that the dual-layer arbiter arbitrates access using round-robin arbitration wherein the refresh controller and the first overlay engine are given equal priority for accessing the SRAM or the DRAM, or using priority arbitration wherein the refresh controller is given higher priority that the first overlay engine for accessing the SRAM or the DRAM. However, Kotzur describes a dual-layer arbiter (504, Figure 5A; Col. 18, lines 53-55) that arbitrates access using round-robin arbitration (Col. 2, line 58-Col. 3, line 29; Col. 19, lines 3-5; Col. 28, line 64-Col. 29, line 25) wherein the refresh controller (210, Figure 4) and other ports are given equal priority for accessing the SRAM (650, Figure 6) or the DRAM (638).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Schlapp, APA, Lavelle, and Rodgers so that the dual-layer arbiter arbitrates access using round-robin arbitration wherein the refresh controller and the first overlay engine are given equal priority for accessing the SRAM or the DRAM, or using priority arbitration wherein the refresh controller is given higher priority that the first overlay engine for accessing the SRAM or the DRAM as suggested by Kotzur because Kotzur suggests the advantage of providing an efficient system for determining priority for selecting and for servicing multiple ports (Col. 2, lines 38-40). Round-robin arbitration is well-known in the art and widely used. Using priority mode is advantageous for making the system more efficient for systems that must service events in a hierarchical fashion and where the service of specific events must be completed before bus mastership is given up. Using round-robin arbitration is

advantageous for making the system more efficient for systems where all masters perform tasks that are of equal priority and the servicing of events can be arbitrarily started and stopped without a problem. This is well-known in the art and can be found in many publications, such as Rynearson's paper.

20. With regard to Claim 12, Schlapp describes a refresh controller request signal, generated by the refresh controller (340, Figure 3; Col. 2, lines 8-12; Col. 13, lines 55-56) and sent to the dual-layer arbiter (330; Col. 13, line 55-Col. 14, line 9), for requesting access to the SRAM (56, Figure 2; Col. 3, lines 26-29) or to the DRAM (Col. 3, lines 21-25) by the refresh controller (Col. 4, lines 27-35). Since the refresh controller accesses both the DRAM and the SRAM, the refresh controller must inherently generate a refresh controller type signal for indicating when access to the SRAM is requested or when access to the DRAM is requested. Schlapp describes a first graphics engine request signal, generated by the first graphics engine (70, Figure 1) and sent to the dual-layer arbiter for requesting access to the SRAM or to the DRAM by the first graphics engine (Col. 3, line 60-Col. 4, line 19). Since the first graphics engine accesses both the DRAM and the SRAM, the first graphics engine must inherently generate a first graphics engine type signal and send it to the dual-layer arbiter, for indicating when access to the SRAM is requested or when access to the DRAM is requested.

However, Schlapp does not teach that the first graphics engine is an overlay engine. However, Lavelle describes that the first graphics engine is an overlay engine, as discussed in the rejection for Claim 9.

21. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of APA [0001-0008], further in view of Lavelle (US006812929B2), further in view of Rodgers (US006131140A), further in view of Kotzur (US006389480B1), further in view of Kato (US006070205A).

Schlapp, APA, Lavelle, Rodgers, and Kotzur are relied upon for the teachings as discussed above relative to Claim 12. Schlapp describes a refresh controller (340, Figure 3; Col. 2, lines 8-12; Col. 13, lines 55-63) that accesses the DRAM and the SRAM (56, Figure 2) (Col. 4, lines 27-25; Col. 13, line 55-Col. 14, line 9).

However, Schlapp, APA, Lavelle, Rodgers, and Kotzur do not teach grant signals. However, Kato describes a DRAM refresh controller (1315, Figure 8) and a DRAM (1305) connected to the first bus (1317) (Col. 9, lines 2-5) and a data retention circuit or refresh controller for SRAM and a SRAM (132) connected to the second bus (1319) (Col. 9, lines 28-34), and a graphics engine (1302) that is connected to both the first and second buses (Col. 8, line 64-Col. 9, line 2). Kato describes first and second bus grant signals generated by the dual-layer arbiter (1306, 1307; Col. 7, lines 23-24; Col. 9, lines 21-26). Therefore, the dual-layer arbiter (1307) generates a second bus grant signal (Col. 9, lines 6-8) and sends it to the refresh controller, to indicate that the refresh controller may access a requested memory (Col. 9, lines 21-34), and therefore the second bus grant signal is a refresh controller grant signal. The dual-layer arbiter (1306) generates a first bus grant signal (Col. 9, lines 6-8) and sends it to the first graphics engine, to indicate that the first graphics engine may access a requested memory (Col. 8, line 64-Col. 9, line 2), and therefore the first bus grant signal is a first graphics engine grant signal.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Schlapp, APA, Lavelle, Rodgers, and Kotzur to include grant signals as suggested by Kato because Kato suggests that grant signals are needed so that a refresh controller or a first overlay engine knows when they may access a requested memory (Col. 7, lines 23-24; Col. 9, lines 2-26). Grant signals are well-known in the art and widely used.

22. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of APA [0001-0008], further in view of Lavelle (US006812929B2), further in view of Rodgers (US006131140A), further in view of Kotzur (US006389480B1), further in view of Laksono (US006288729B1).

Schlapp, APA, Lavelle, Rodgers, and Kotzur are relied upon for the teachings as discussed above relative to Claim 11. Lavelle describes that the graphics engine is an overlay engine for manipulating the graphics data, as discussed in the rejection for Claim 9. Rodgers describes a first mux and a second mux, as discussed in the rejection for Claim 4. Schlapp describes a dual-layer arbiter that grants access of a graphics engine to the SRAM and a second select signal further indicates when the graphics engine is granted access to the DRAM by the dual-layer arbiter, as discussed in the rejection for Claim 10.

However, Schlapp, APA, Lavelle, Rodgers, and Kotzur do not teach a second graphics engine. However, Laksono describes a second graphics engine, as discussed in the rejection for Claim 8.

Allowable Subject Matter

23. Claims 15, 16, and 18-20 are allowed.

24. The following is a statement of reasons for the indication of allowable subject matter:

The prior art taken singly or in combination do not teach or suggest a dual-memory arbitrated graphics sub-system comprising dynamic-random-access memory (DRAM) means for storing graphics data; static random-access memory (SRAM) means for storing display pixels in a frame buffer; refresh controller means for reading the display pixels from the frame buffer and writing the display pixels to a display during a screen refresh; wherein the DRAM means is further for storing extension pixels in an extended frame buffer read by the refresh controller means; first overlay engine means for processing the graphics data to generate display pixels or intermediate graphics data; second overlay engine means for processing the graphics data to generate display pixels or intermediate graphics data; arbiter means, receiving first requests for access of the SRAM means from the refresh controller means, the first overlay engine means, or the second overlay engine means, for arbitrating among the first requests when received at a same time period to generate a first grant to a first winning requestor, and for arbitrating among the second requests when received at a same time period to generate a second grant to a second winning requestor, the arbiter means allowing simultaneous access of the SRAM means by the first winning requestor and the DRAM means by the second winning requestor. Applicant states that means-plus-function claims are intended to cover not only the structures described in the specification for performing the function and their structural equivalents, but also equivalent structures [0058]. Therefore, the arbiter means includes the functions detailed in the

specification, and these functions include that the dual-layer arbiter has three requestors, and each requestor has a pair of request-grant lines that carry request-grant handshake signals [0033]. The first bus means for transferring address and data to the SRAM means; second bus means for transferring address and data to the DRAM means. The bus means includes the functions detailed in the specification, and these functions include that individual signals in the two buses are kept separate at any particular time, but routing area and other bus resources may be shared [0032]. First selector means, coupled to the first bus means, for selecting the refresh controller means, the first overlay engine means, or the second overlay engine means for connection to the first bus means in response to an indication of the first winning requestor from the arbiter means. The arbiter means includes the functions detailed in the specification, and these functions include that when the refresh controller wins arbitration, that means that there are no other requestors to DRAM, and the arbiter drives SEL_A to indicate that the mux 42 selects lines from the refresh controller to connect to the first bus and the SRAM [0034]. Once the mux 42 has connected the refresh controller to the first bus, another set of handshake signals between the arbiter and the two-layer bus matrix help perform the memory access. The arbiter activates the grant line to indicate that the first bus is ready to begin access. The two-layer bus matrix responds with a ready signal RDY_A when the SRAM is ready to allow access [0035]. Second selector means, coupled to the second bus means, for selecting the refresh controller means, the first overlay engine means, or the second overlay engine means for connection to the second bus means in response to an indication of the second winning requestor from the arbiter means, whereby three requestors are arbitrated for access of two memories, as recited in Claim 15. The second selector means includes the functions detailed in the specification, and these functions include that a

control signal SEL_B from the arbiter controls mux 44 and the two-layer bus matrix, which generates RDY_B as an acknowledgement back to the arbiter. First and second video overlay engines also generate request handshake signals REQ_VO1, REQ_VO2 and receive grant handshake signals GNT_VO1, GNT_VO2 from the arbiter [0036]. Since Claim 15 is allowable, Claims 16 and 18-20 are also allowable since they depend from Claim 15.

Prior Art of Record

"Multiplexer." http://en.wikipedia.org/wiki/Multiplexer.

"Video Overlay." http://www.webopedia.com/TERM/V/video_overlay.html.

Rynearson, John. "VMEbus System Controller." July 1997. VITA Journal. http://www.vita.com/vme-faq/systemcontroller.html.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella can be reached on 571-272-7778. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

ULKA J. CHAUHAN
PRIMARY EXAMINER